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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,063	05/09/2006	Catherine Robert	S1022.81243US00	1852

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EXAMINER	
MOLL, JESSE R	

ART UNIT	PAPER NUMBER
2181	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/535,063	ROBERT ET AL.	
	Examiner	Art Unit	
	JESSE R. MOLL	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Floyd et al. (U.S. Patent No. 6,961,875) herein referred to as Floyd in view of Cheon (U.S. Patent Application No. 6,070,210), herein referred to as Cheon'210.

Referring to claim 1, Floyd discloses, as claimed, a method comprising: transmitting first digital messages to an analysis tool (Trace array 207; see fig. 2; col. 4, lines 20-25) from a monitoring circuit (Counter 202) representative of first specific events (such as the event sequence signal 217; see fig. 2; col. 59-65) which depend on execution of an instruction sequence by a microprocessor (see col. 4, lines 23-27 regarding signals 212), integrated to the microprocessor; detecting, with a request circuit (such as event sequence logic 232; see fig. 2), at least one second specific event (start signal 218) independent from the execution of the instruction sequence by the microprocessor; transmitting to the monitoring circuit (Counter 202), when the at least one second specific event is detected (see col. 4, lines 59-63), a characteristic data

signal (event sequence signal 217) associated with said at least one second specific event; storing the characteristic data signal (inherently, the signal must be stored; at least temporarily on the wire between 232 and 202) in the monitoring circuit and transmitting at least one second digital message representative of the stored characteristic data signal to the analysis tool (address 204 through address decoder 203; see fig. 2, col. 4 , lines 43-50); and processing the first digital messages and the at least one second digital message via the analysis (determining where to store input logic signals 205; see col. 4, lines 43-50) tool to analyze operation of the microprocessor , including determining the instruction sequence executed by the microprocessor (as an instruction trace, see col. 4, lines 19-25), and the at least one second specific event (the address; as stated above).

Floyd does not expressly disclose if resource management conditions are fulfilled, transmitting an acknowledgement signal to the request circuit.

Cheon '210 teaches if resource management conditions are fulfilled (such as in the situation when memory 10 is available for being written), transmitting an acknowledgement signal (through DACK, see Fig. 2) to the request circuit.

It would have been obvious for one of ordinary skill in the art at the time of the invention to have modified the invention of Floyd by modifying the communication between counter 202 and event sequence logic 232 by implementing a protocol wherein if resource management conditions are fulfilled, transmitting an acknowledgement

signal to the request circuit (as taught by Cheon '210) to yield predictable results in order to increase performance by using a flexible communication protocol.

Claim 5 recites equivalent limitations as claim 1, but is claimed as an apparatus. Claim 5 is rejected as the apparatus using the method of claim 1.

As to claim 2, Cheon'210 also discloses the resource management conditions are fulfilled when the monitoring circuit (DMA device 100, see Fig. 2) is not transmitting digital messages representative of the first specific events (note this is in the situation when DMA device is available to be used).

As to claim 3, Cheon'210 also discloses the digital message representative of the stored data signal comprises an identifier (such as valid/invalid bit) and the characteristic data signal (the data bits).

As to claim 4, Cheon'210 also discloses the characteristic data (DATA) signal corresponds to the values on input terminals (such as the MBR for CPU connecting the data bus in the Cheon'210's system) of the microprocessor (200, see Fig. 2).

As to claim 6, Cheon'210 also discloses the request circuit (such as ALU in the CPU of the Cheon'210's system), the monitoring circuit (SCSI controller 120, see Fig. 2), the monitoring circuit (DMA device 100, see Fig. 2), and the microprocessor are integrated in a same chip (see Fig. 2).

As to claim 7, Cheon'210 also discloses the detection means (such as ALU in the CPU of the Cheon'210's system) is connected to input terminals (such as the MBR for

CPU connecting the data bus in the Cheon'210's system) of the microprocessor (200, see Fig. 2).

Response to Arguments

1. Applicant's arguments filed 6 May 2008 regarding the rejection of claims 1-7 under 35 USC 102 have been fully considered but they are moot in view of the new grounds of rejection presented above.

2.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571)272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

/J. R. M./
Examiner, Art Unit 2181

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181